## 20.2 A Digitally Calibrated 5.15 - 5.825GHz Transceiver for 802.11a Wireless LANs in 0.18μm CMOS

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The trend towards low cost integration of wireless systems has driven the introduction of innovative single chip radio architectures in CMOS technologies as an inexpensive alternative to the traditional superheterodyne bipolar implementations. This work describes a 0.18μm CMOS direct conversion transceiver, part of a two-chip solution implementing both PHY and MAC for 802.11a.

Although attractive as a highly integrated solution, direct conversion architecture suffers from problems such as DC offsets, flicker noise and poor quadrature matching, that are further aggravated by using CMOS technology [1]. Furthermore, the 802.11a standard high bit-rate modes require closely matched I/Q frequency response. To alleviate those limitations, a transceiver topology allowing the use of the companion digital chip for calibration, has been implemented as shown in Fig. 20.2.1. Both transmitter and receiver use direct conversion and employ fully differential signal paths. By adding loop-back switches, the DC offset, TX and RX I/Q gain mismatch and I/Q frequency response can be independently calculated and corrected during the idle time between frames or at power-up.

The balanced low noise amplifier (LNA) shown in Fig. 20.2.2 uses an NMOS cascoded differential pair with inductive degeneration. On-chip spiral inductors are used, except for the input matching network, which uses bond-wire inductors. Two gain settings of 16dB/10dB are provided. At the high gain setting, the LNA has a noise figure of 3.2dB. Input matching is wideband, to cover all three 802.11a bands. The output of the LNA is demodulated directly into baseband by a quadrature demodulator, based on the mixer shown in Fig. 20.2.2. A folded current signal path using PMOS switches reduces flicker noise. The mixer features 10dB of gain and a noise figure of less than 12dB. The overall receive chain path DC offset is calculated, tracked digitally, and real-time corrected at the output of the RX mixers by two independent 8-bit current steering digital-to-analog converters (DACs).

The baseband path of the receiver consists of two programmable gain amplifiers (PGA), a low-pass filter and an output buffer. The first PGA employs a low-noise, high dynamic range single-stage amplifier, while the second is an operational amplifier-based feedback gain stage. The composite gain varies from 2dB to 53dB, programmable in 3dB steps. The fourth-order Chebyschev filter cell used for channel selection is implemented as a cascade of two biquads. It employs Gm-OTA-C integrators based on the regulated cascode topology, as shown in Fig. 20.2.3 and is tuned by the DC voltage Vc generated by an 8-bit DAC. During transceiver calibration, the responses of both I and Q paths are independently measured and corrected. I-path is measured from the feedback path formed by switches SW5-SW1, while Q-path is from SW5-SW2. A calibration sequence generated digitally is used to set the bandwidth to 9MHz. Residual mismatch along the pass-band of the filters is measured and compensated digitally. The output of the receiver is digitized by dual 10-bit, 40MHz analog-to-digital converters on the digital companion chip.

The direct up-conversion transmit path consists of I/Q filters, a programmable gain modulator (PGM) and an RF driver amplifier. The input signal is generated by dual 10-bit 40MHz DACs located at the digital companion chip. The filters are identical to the ones used in the receiver and are calibrated digitally using the feedback path formed by switches SW3 and SW4. The PGM core cell is a folded cascode Gilbert mixer, while the output driver is a cascoded differential pair. A programmable gain amplifier that utilizes a resistive ladder at the input of the mixers provides 27dB programmable attenuation in 3dB steps. Finally, the driver amplifier is a single stage differential pair, inductively degenerated to improve linearity and delivering 0dBm of output power into a 50Ω differential load.

An integer-N PLL using a third-order passive loop filter generates the LO signal at half the desired frequency, in order to minimize VCO pulling and avoid interference with the RF signal. The reference frequency for the loop is 10MHz and 2.5MHz, for the lower and upper 802.11a bands, respectively. The programmable divider in the feedback loop is formed by cascaded 2/3 dividers giving division ratios of $2^n$ to $2^n$-1, where n is the number of stages used. A charge-pump employing a replica bias circuit helps achieve low in-band phase noise and spurs below –65dBc at a 10MHz offset. The VCO uses a complementary pair of negative resistor structures and MOS varactors operating in accumulation mode for tuning. Its output is multiplied by a Gilbert cell-based doubler, and quadrature signals are generated by second-order polyphase filters. Two different VCO/doubler/polyphase filter combinations cover the three 802.11a bands. Active RF switches select the appropriate LO. The synthesizer achieves phase noise better than –115dBc/Hz at 1MHz offset and integrated phase noise of less than $0.8^o$ from 1kHz to 10MHz (Fig. 20.2.4).

Closed-loop TX power control, through an external envelope detector, is also used to measure the transmitter IQ mismatch and remove it using digital pre-distortion [2]. Measurements show that sideband suppression better than 50dB can be achieved. Using the calibrated transmit path, the receive path I/Q mismatch can be measured and compensated digitally by closing the internal loop-back formed by switch SW6. Figure 20.2.5 shows the received constellation for the 802.11a 54Mb/s mode. Sensitivity better than –70dBm can be achieved at the input of the reference board.

The transceiver was implemented on 0.18μm CMOS and occupies a total silicon area of 18.5mm$^2$. A die microphotograph is shown in Fig. 20.2.7. Measurement results are summarized in Fig. 20.2.6. The receiver features a NF of 5.5dB at maximum gain, while input $P_{-1dB}$ is better than –20dBm at minimum gain. Power consumption is 250mW in receive mode and 300mW during transmit.

*Acknowledgements*
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*References*
[1] P. R. Gray and R.G. Meyer, "Future Directions in Silicon ICs for RF Personal Communications," Proc. IEEE Custom Integrated Circuits Conference, pp. 83-90, May 1995.
[2] J. K. Cavers, "New Methods for Adaptation of Quadrature Modulators and Demodulators in Amplifier Linearization Circuits," *IEEE Transactions on Vehicular Technology*, vol. 46, no. 3, pp. 707-716, Aug. 1997.

 

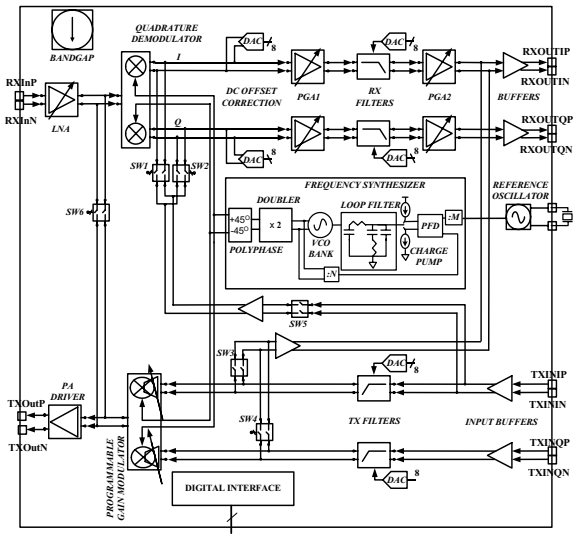


Figure 20.2.1: Transceiver block diagram.

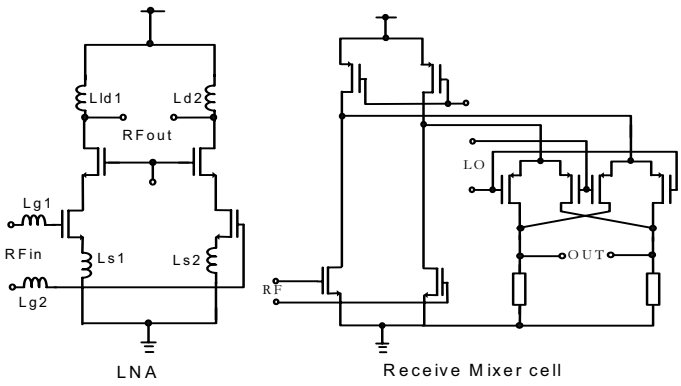


Figure 20.2.2: LNA + RX Mixer.

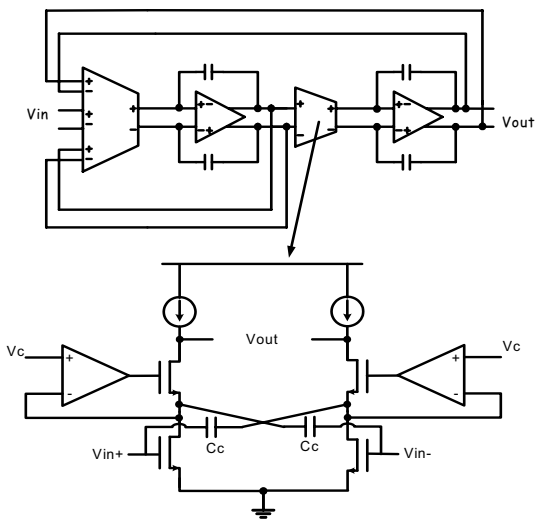


Figure 20.2.3: Biquad and transconductor.

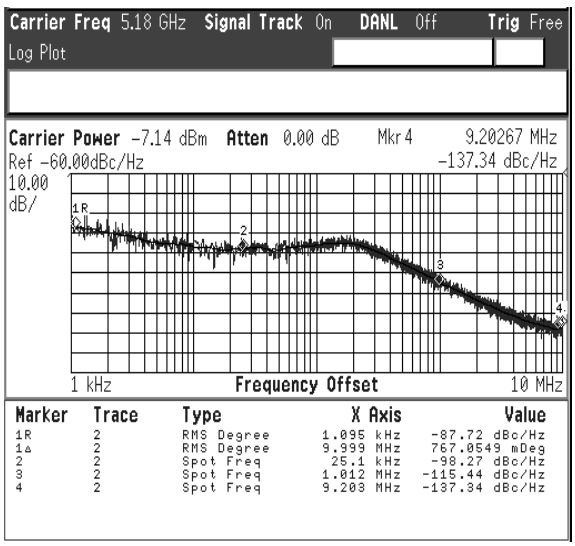


Figure 20.2.4: PLL phase noise.

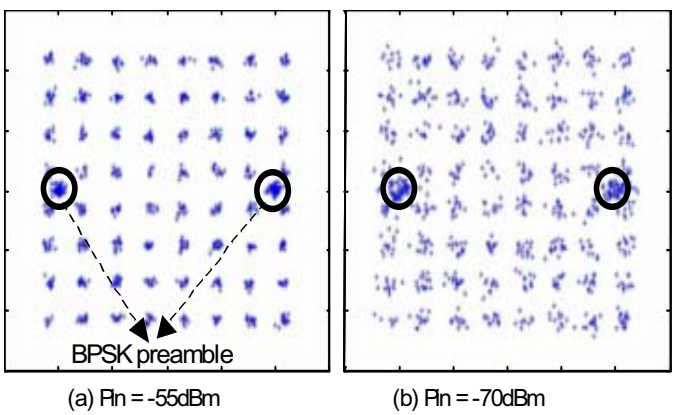


Figure 20.2.5: Received constellation after calibration.

| | |
|---|---|
| VDD | 1.8 V |
| TX mode power dissipation | 302mW |
| RX mode power dissipation | 248mW |
| RX Chain path noise figure | 5.5dB |
| RX Chain path max gain | 77dB |
| RX Chain path min gain | 20dB |
| RX path IIP3 (max gain, two tones Fc+20MHz, Fc+40MHz) | -17dBm |
| RX path P-1dB (min gain) | -20dBm |
| SSB Phase noise (1MHz offset) | -115dBc |
| Integrated Phase noise (DSB, 1kHz – 10MHz) | -37.4dBc |
| Supported bands | 5.15GHz – 5.35GHz<br>5.725GHz – 5.825GHz |
| TX output P-1dB | 0dBm |
| Technology | 1P6M CMOS 0.18µm |
| Die Size | 4.5mm x 4.1mm |
| Package | MLF-64 |

Figure 20.2.6: Performance summary.

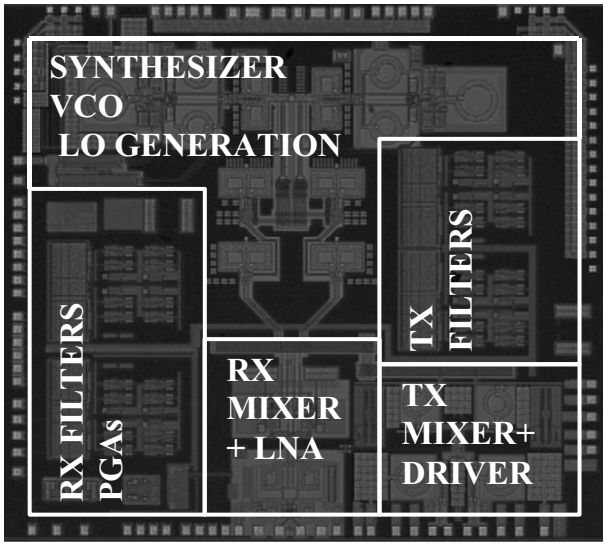


**Figure 20.2.7: Chip microphotograph.**



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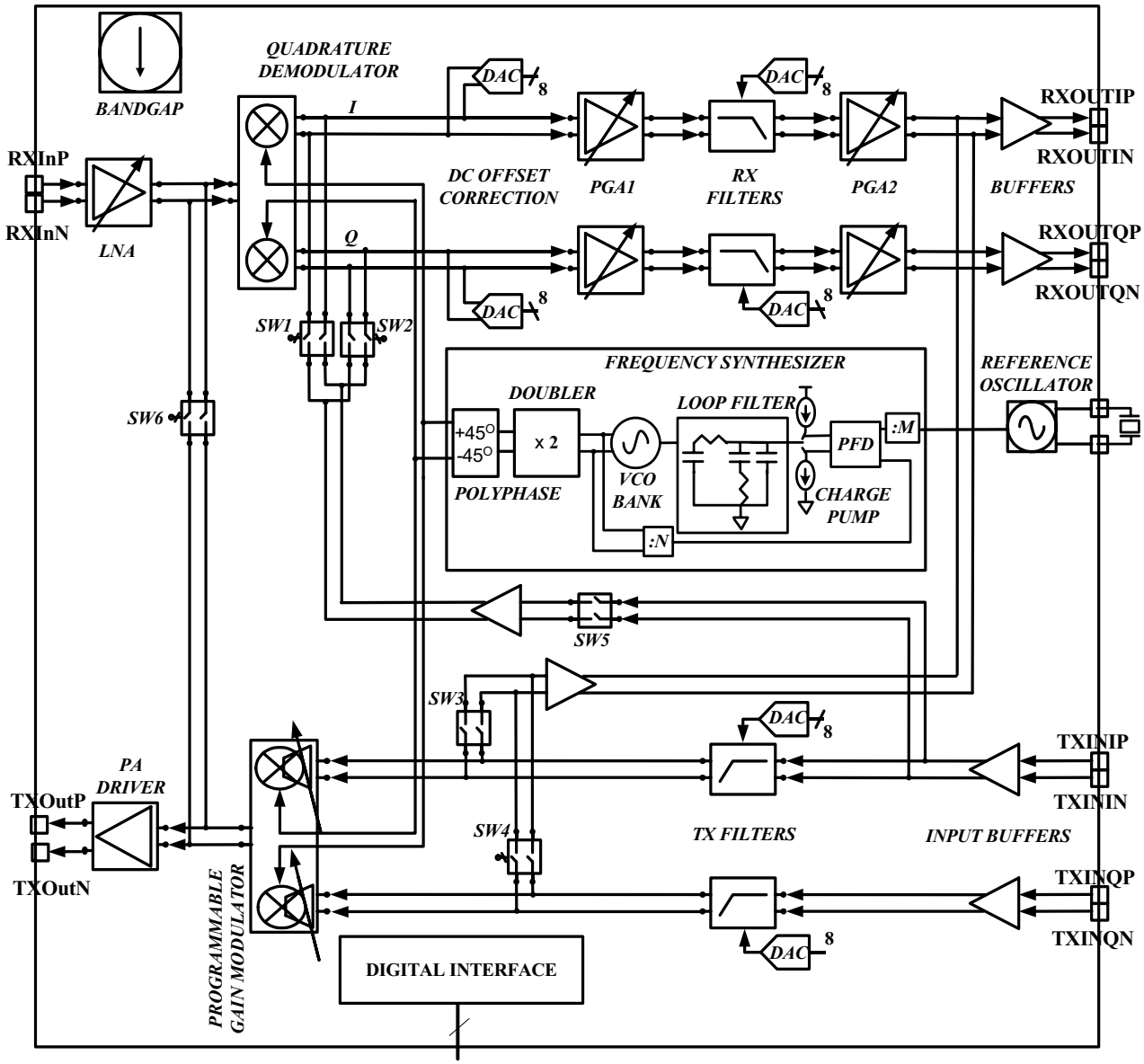


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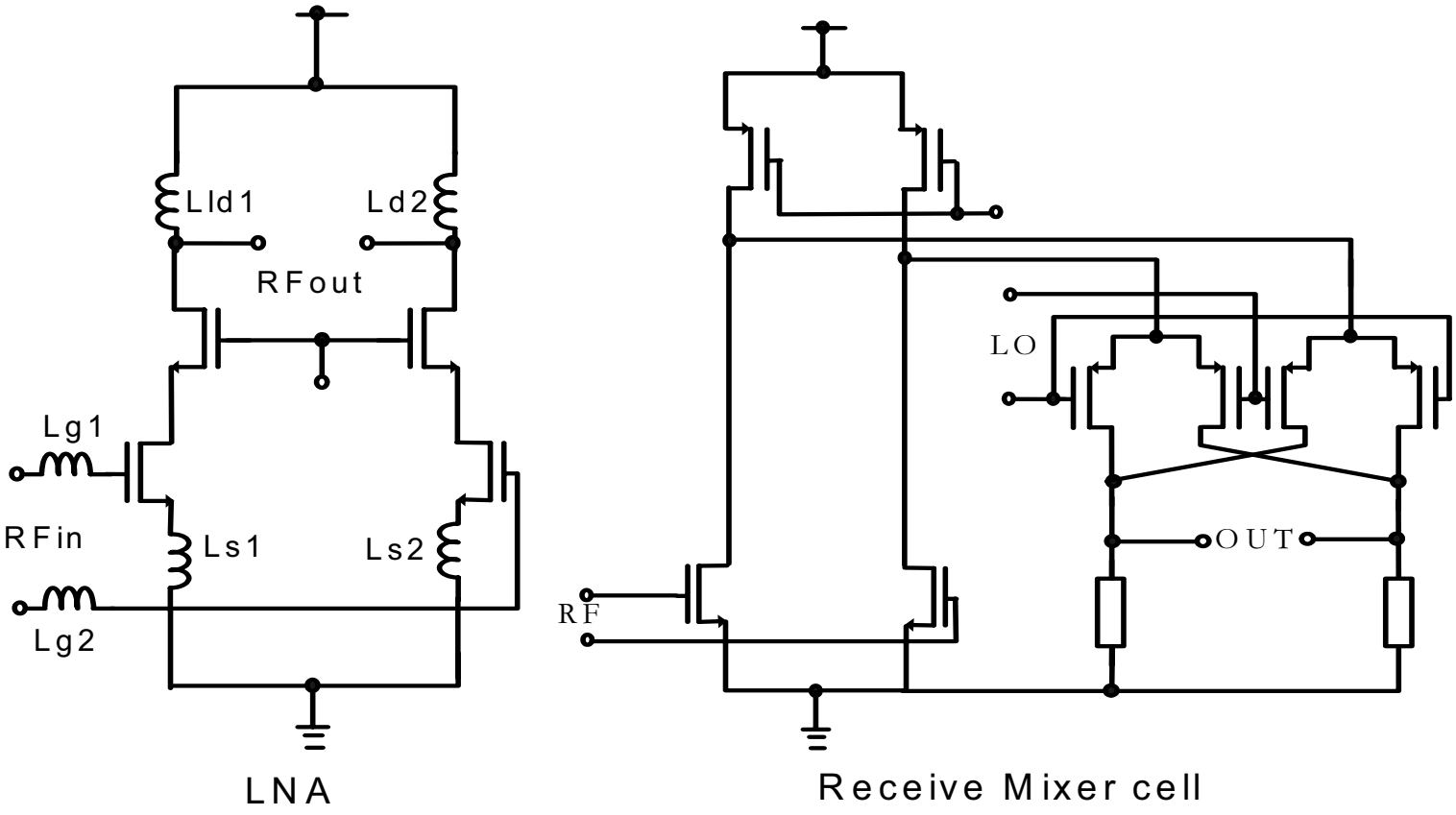
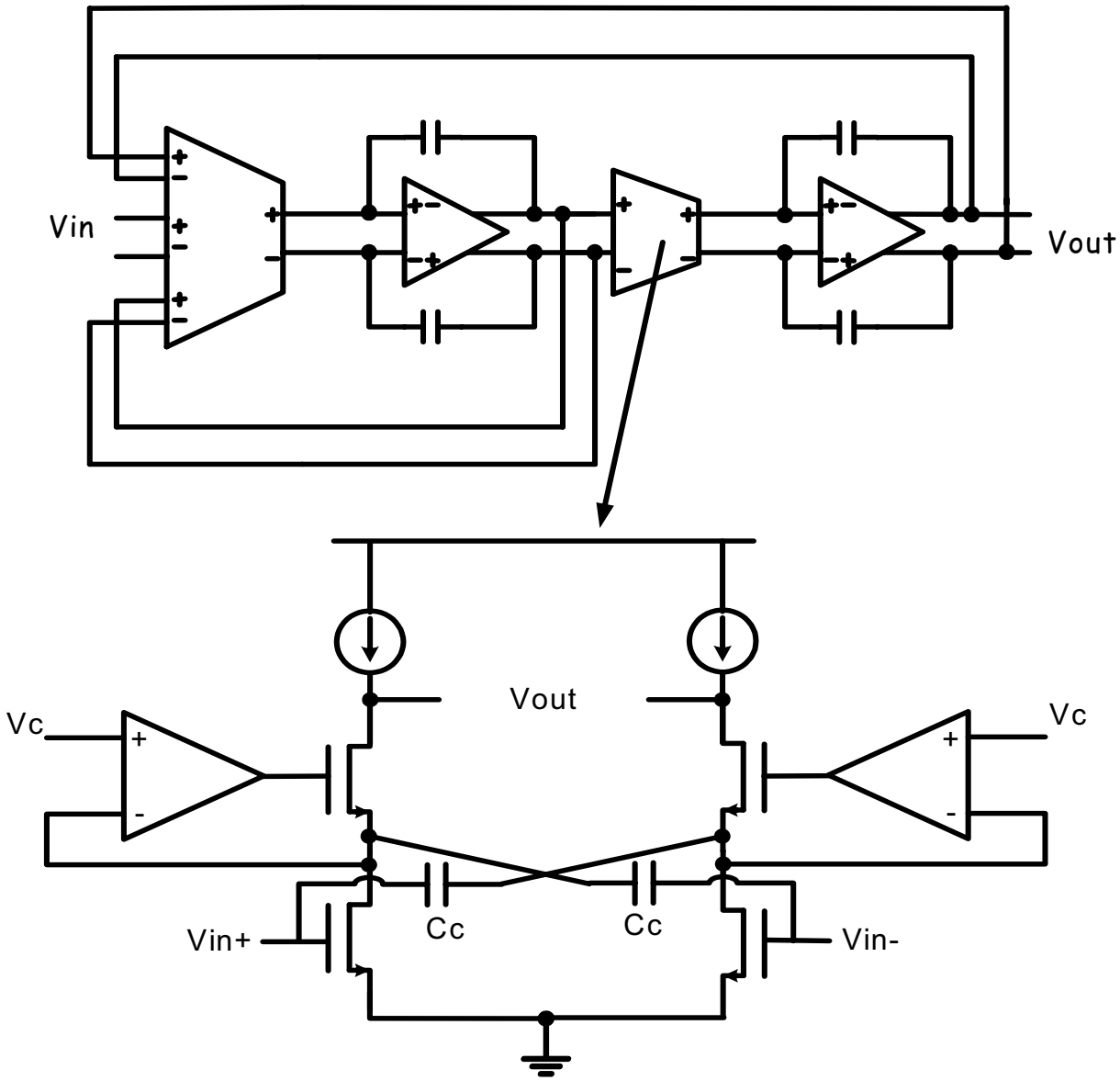



**Figure 20.2.2: LNA + RX Mixer.**

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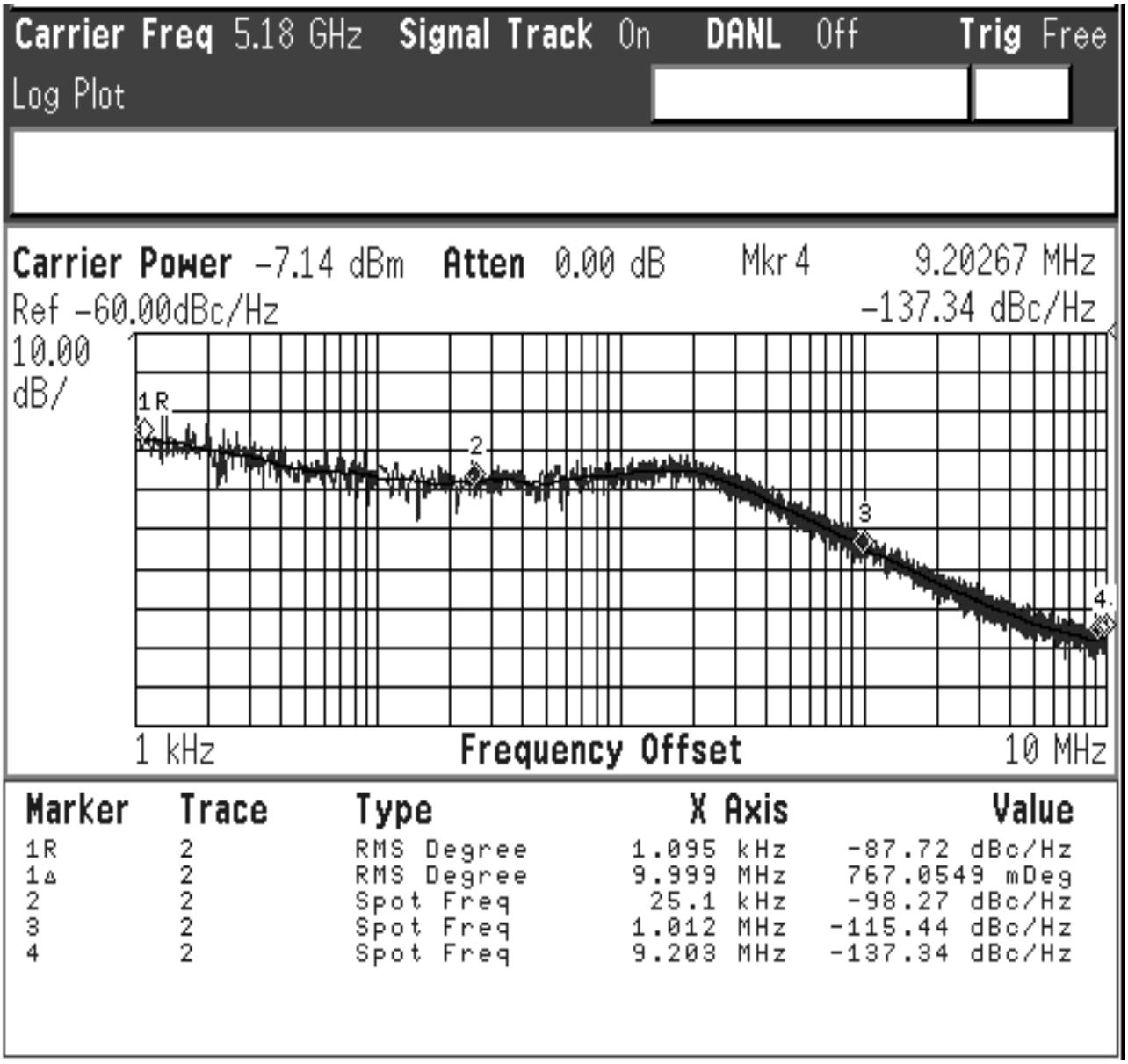


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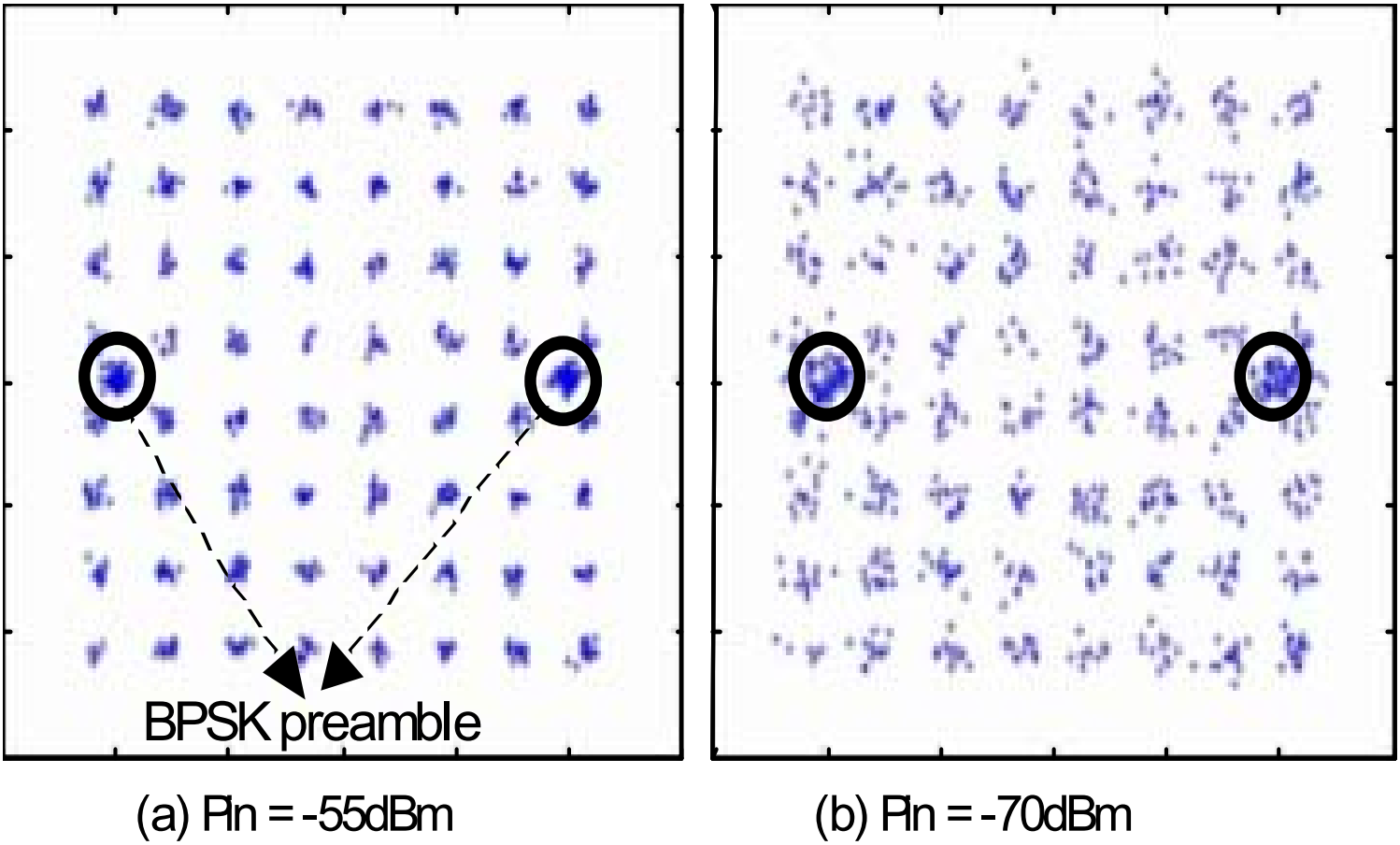


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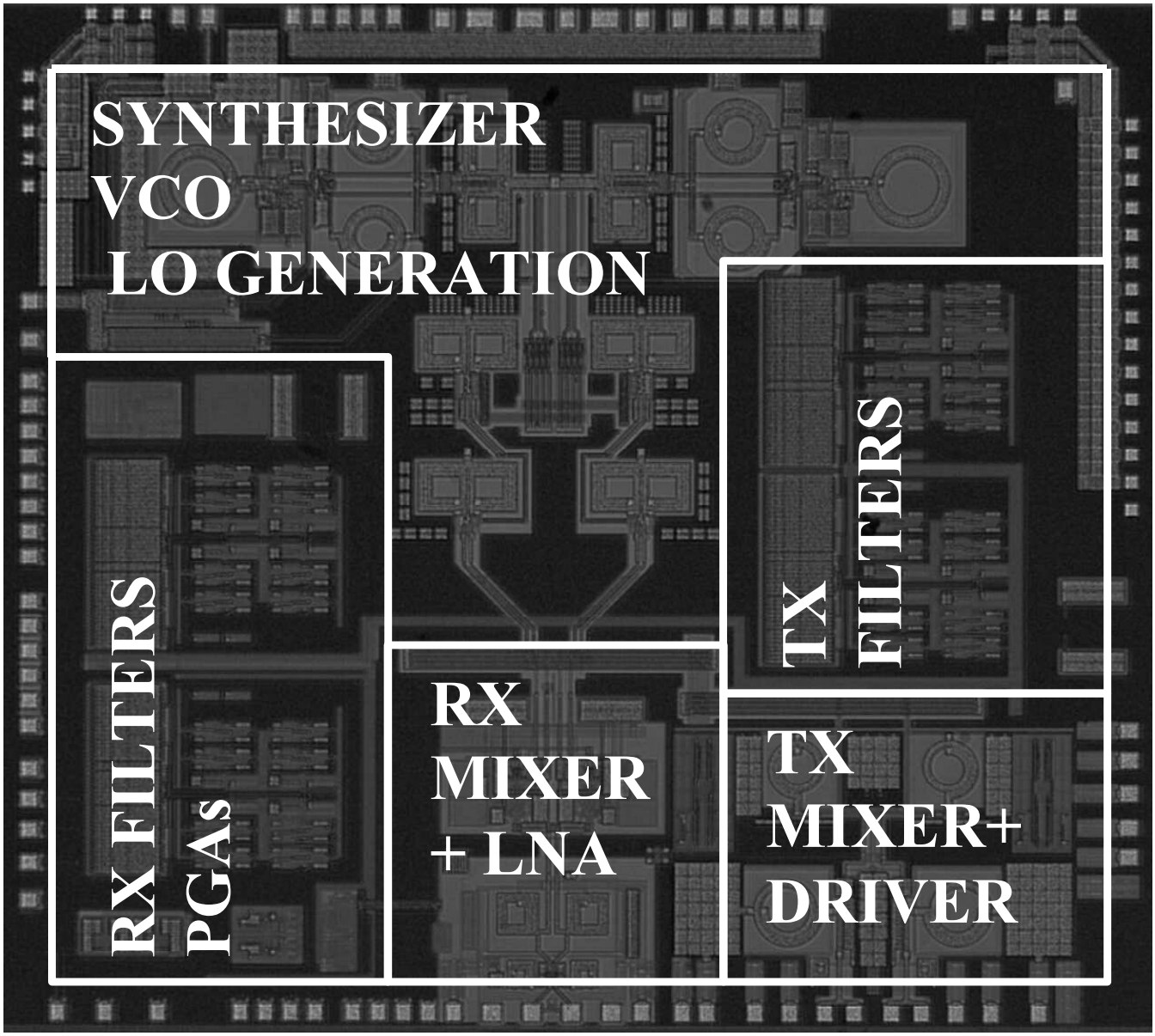


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